ABSTRACT

A semiconductor memory device includes a plurality of memory array blocks including predetermined numbers of memory cells, the memory array blocks being arranged in the row direction; a RAS chain being aligned at a side of the plurality of memory array blocks in the row direction, the RAS chain for selecting and activating a particular word line; a CAS chain being aligned at the other side of the plurality of memory array blocks in the column direction, the CAS chain for amplifying N bits of data from the plurality of memory array blocks and outputting the result to an input/output (IO) line, wherein N is a natural number more than 2; and a data converter for continuously outputting the N bits of data input via the IO line from a memory array block nearest to the RAS chain to a memory array block farthest from the RAS chain.